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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

03103937.3

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Frequency divider

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
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Frequency Divider

The invention relates to a frequency divider.

Frequency dividers are well-known and widely-used devices in applications as Phase Locked Loops (PLLs), prescalers, digital receivers. Normally a frequency divider requires flip-flops coupled in a convenient manner for obtaining a desired frequency division.

The actual trends in semiconductor technology is shrinking transistors size for improving the speed of the circuits and downsize the supply voltages for the integrated circuits for reducing a dissipation power of the chips.

US-A 6,424,194 describes ultra high-speed circuits using current-controlled CMOS (C^3MOS) logic fabricated in conventional CMOS process technology. An entire family of logic elements including inverters/buffers, level shifters, NAND, NOR, XOR gates, latches, flip-flops and the like are implemented using C^3MOS techniques. Optimum balance between power consumption and speed for each circuit application is achieved by combining C^3MOS logic with low power conventional CMOS logic. The combined C^3MOS/CMOS logic allows greater integration of circuits such as high-speed transceivers used in fiber optic communication systems. It is observed that the circuits presented in the above-mentioned patent still use at least two stacked transistors, which make them less suitable for relative low-voltage (1.2, .9 or .7 V) supply applications. By stacking transistors, the threshold voltages of the upper transistors increase due to the back-bias effect. As a consequence, the upper transistors do not have maximum gain and maximum speed of operation.

It is therefore an object of the invention to provide a frequency divider suitable for low-voltage supply voltages and high speed of operation.

The invention is defined in the independent claim. Dependent claims describe advantageous embodiments.

In accordance with the present invention, the frequency divider comprises a first flip-flop having a first clock input for receiving a clock signal, a first data input and a

first output. The divider further comprises a second flip-flop having a second clock input for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input, a second data input coupled to the first output. The second flip-flop further comprises a second output and a third output, the second and third outputs (Q2, Qa2) providing signals that are mutually in anti-phase. The third output is coupled to the first data input. A period of the clock signal is of the same order of magnitude as a delay through an inverted stage of the divider.

A prior art frequency divider is shown in Fig. 2. It comprises first and second flip-flops, each flip-flop, each of them being implemented as shown in Fig. 1. In Fig. 1, transistors M1 and M2 implement a R-S flip-flop, which is controlled by a clock signal having two components that are mutually in anti-phase Cl and $\overline{Cl}$, respectively. An input signal D is inputted via a controlled inverter M5, M6 to an input of the flip-flop. Two flip-flops of this kind are coupled as in Fig. 2 for providing a frequency divider. It is observed that there is a feedback connection from an output of the second flip-flop Q2 via the controlled inverter M5, M6 for providing an input signal Q4 to the first flip-flop M1 – M4. The inverter M5, M6 delays the signal with a time delay depending on its geometry and on the technology used for its implementation. When the signals whose frequency needs to be divided have a period in the same range as the delay through the inverter M5, M6, the signal cannot be transmitted from the input of the controlled inverter to its output. Hence, the controlled inverter M5, M6 at the input limits the maximum frequency, which may be divided. The present invention is based on the inventive recognition that inverting the phase of the feedback signal from the second flip-flop allows for an elimination of the inverter M5, M6 and contributes to an increase of the maximum frequency of input signals, which are divided with this frequency divider.

In an embodiment, a controllable switch is coupled to the first data input and to the third output. The controllable switch is controlled by a clock signal driving the first flip-flop. When the delay through the inverters is not critical but still wants to obtain a frequency divider for relative high frequency signals from the controlled input inverter we remove one transistor and apply a clock signal substantially in phase with the clock signal of the first flip-flop. Hence, the maximum frequency of operation is increased when compared with the state of the art divider because the delay through the switch is smaller than the delay through two transistors implementing the controlled inverter.

Optionally, the controllable switch is coupled to the third output via resistive means. The resistive means reduces the current supplied to the input of the first flip-flop and

the loading due to the input impedance of the first flip-flop. As a direct consequence, the consummated power is reduced.

The above and other features of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a prior-art R-S flip-flop,

Fig. 2 depicts a frequency divider using a prior-art flip-flop,

Fig. 3 depicts a frequency divider according to an embodiment of the invention, and

Fig. 4 depicts a frequency divider according to another embodiment of the invention.

Fig. 3 depicts a frequency divider according to an embodiment of the invention.

The frequency divider comprises a first flip-flop M1, M2, M3, M4 having a first clock input $\overline{Cl}$ for receiving a clock signal. The flip-flop further comprises a first set input Q4 and a first non-inverted output Q1. The frequency divider further comprises a second flip-flop M1', M2', M3', M4' having a second clock input Cl for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input $\overline{Cl}$, a second set input coupled to the first non-inverted output Q1, a second non-inverted output Q2 and a second inverted output $\overline{Q2}$, the second inverted output $\overline{Q2}$ being coupled to the first set input Q4. A period of the clock signal is of the same order of magnitude as a delay through an inverter stage of the divider.

In current CMOS technology the circuits used for frequency division are implemented in Current Mode Logic (CML) and specifically in Source Coupled Logic (SCL). When it is necessary to divide a signal having a relatively high frequency, e.g. 10 GHz current CMOS logic circuits are not suitable because it is necessary to have a relative low supply voltage for limiting the power dissipation. In these conditions, the necessary current sources for CML or SCL circuits suffer from a relatively large drain-to substrate capacitance of the MOS transistors. The frequency divider shown in Fig. 3 eliminates an inverter from the input of the used flip-flops. Because the inverter phase shifts the input

signal with 180 degrees it is necessary to invert the input signal for obtaining the same division function as the prior-art divider. Hence, the input of the first flip-flop is coupled to the inverted output $\overline{Q2}$ of the second flip-flop, which provides a signal substantially in anti-phase i.e. phase shifted over 180 degrees with respect to the signal provided by the second output Q2.

When the frequency of the clock signal Cl is substantially different from the delay through inverters implementing flip-flops, a controllable switch M7 is coupled to the first data input Q4 and to the third output Qa2. The switch is controlled by a clock signal driving the first flip-flop M1, M2, M3, M4. The maximum frequency of operation is increased when compared with the state of the art divider because the delay through the switch is smaller than the delay through two transistors implementing the controlled inverter. The controllable switch M7 may be coupled to the third output Qa2 via resistor R. The resistor R reduces the current supplied to the input of the first flip-flop and the loading due to the input impedance of the first flip-flop. As a direct consequence, the consummated power is reduced.

It should be mentioned here that the pairs of transistors M1, M4; and M2, M3 in Figs. 1 - 4 are in fact controlled inverters.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference signs in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A frequency divider comprising:

- a first flip-flop (M1, M2, M3, M4) having a first clock input ($\overline{Cl}$) for receiving a clock signal, the flip-flop further comprising a first set input (Q4) and a first non-inverted output (Q1), and

- a second flip-flop (M1', M2', M3', M4') having a second clock input (Cl) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input ($\overline{Cl}$), a second set input coupled to the first non-inverted output (Q1), a second non-inverted output (Q2) and a second inverted output ($\overline{Q2}$), the second inverted output ($\overline{Q2}$) being coupled to the first set input (Q4).

2. A frequency divider as claimed in Claim 1, wherein a period of the clock signal is of the same order of magnitude as a delay through an inverter stage of the divider.

3. A frequency divider as claimed in Claim 1, wherein a controllable switch (M7) is coupled to the first data input (Q4) and to the third output (Qa2) and being controlled by a clock signal driving the first flip-flop (M1, M2, M3, M4).

4. A frequency divider as claimed in Claim 1, wherein the controllable switch (M7) is coupled to the third output (Qa2) via resistive means (R).

ABSTRACT:

A frequency divider comprising a first flip-flop (M1, M2, M3, M4) having a first clock input ($\overline{Cl}$) for receiving a clock signal, the flip-flop further comprising a first set input (Q4) and a first non-inverted output (Q1). The frequency divider further comprises a second flip-flop (M1', M2', M3', M4') having a second clock input (Cl) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input ($\overline{Cl}$), a second set input coupled to the first non-inverted output (Q1), a second non-inverted output (Q2) and a second inverted output ($\overline{Q2}$), the second inverted output ($\overline{Q2}$) being coupled to the first set input (Q4).

Fig. 3

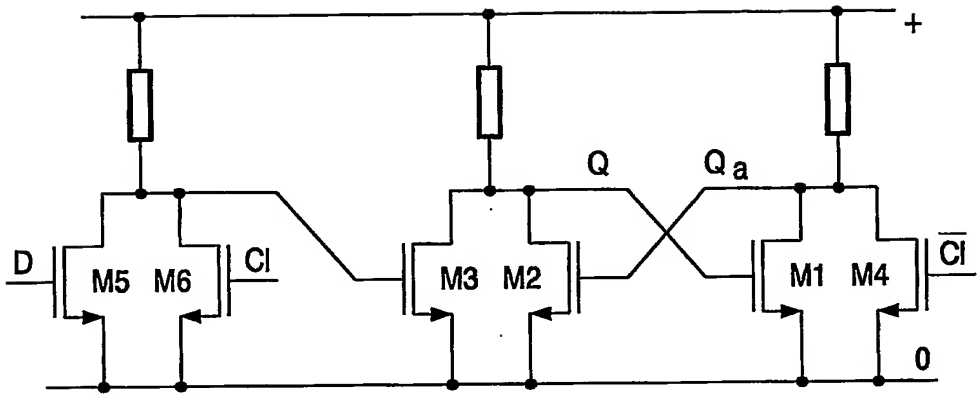

FIG. 1

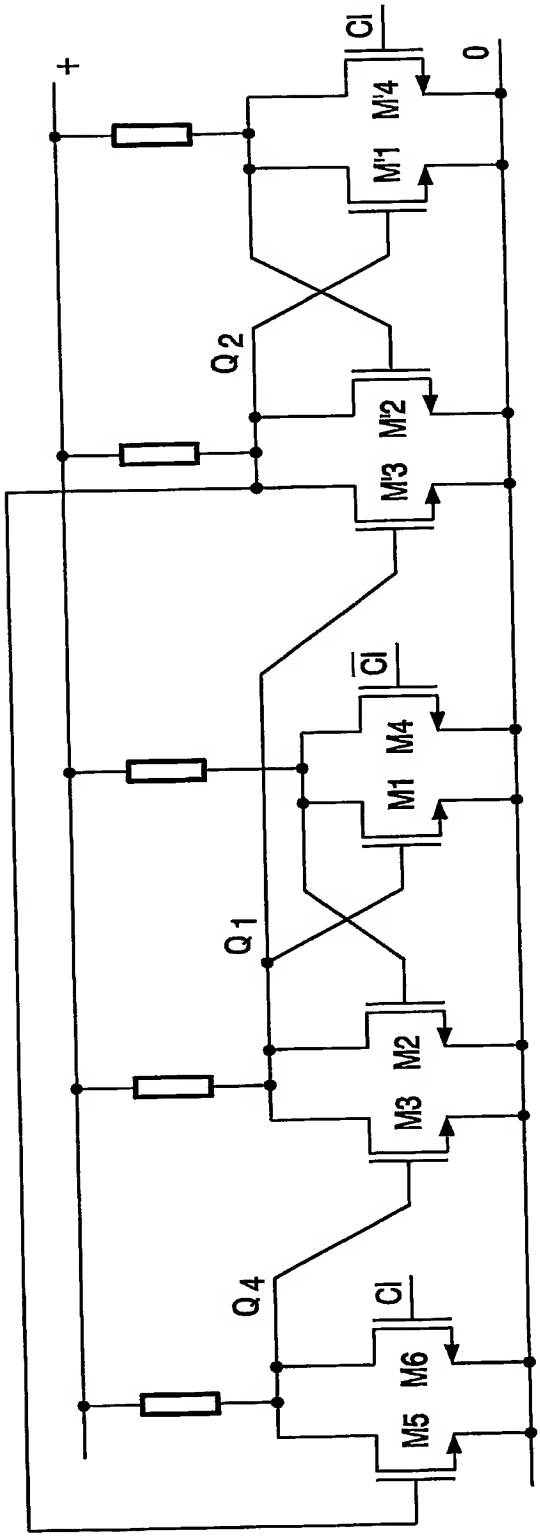

FIG. 2

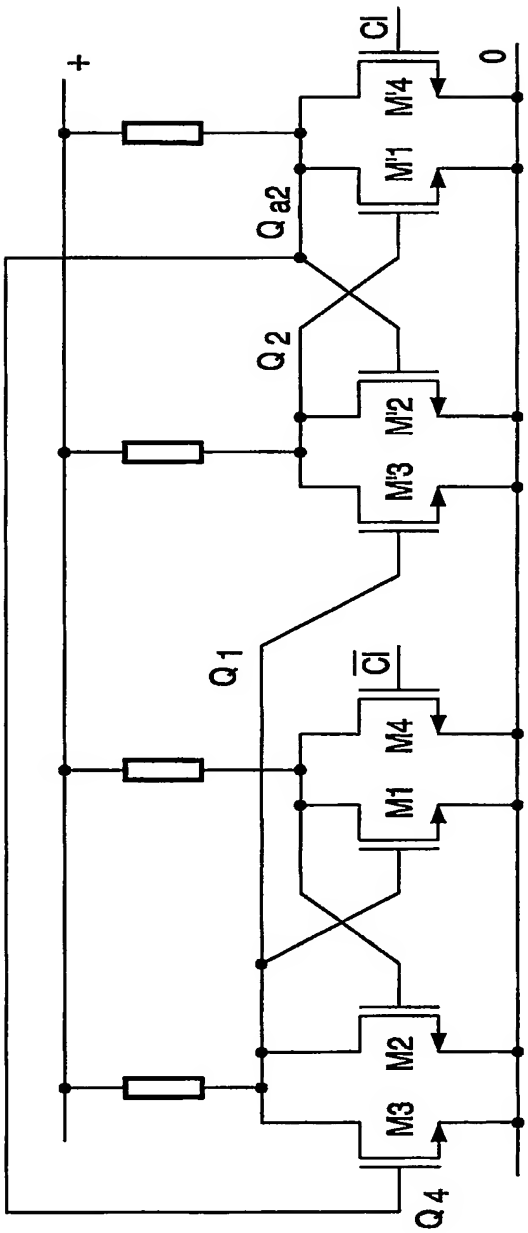

FIG. 3

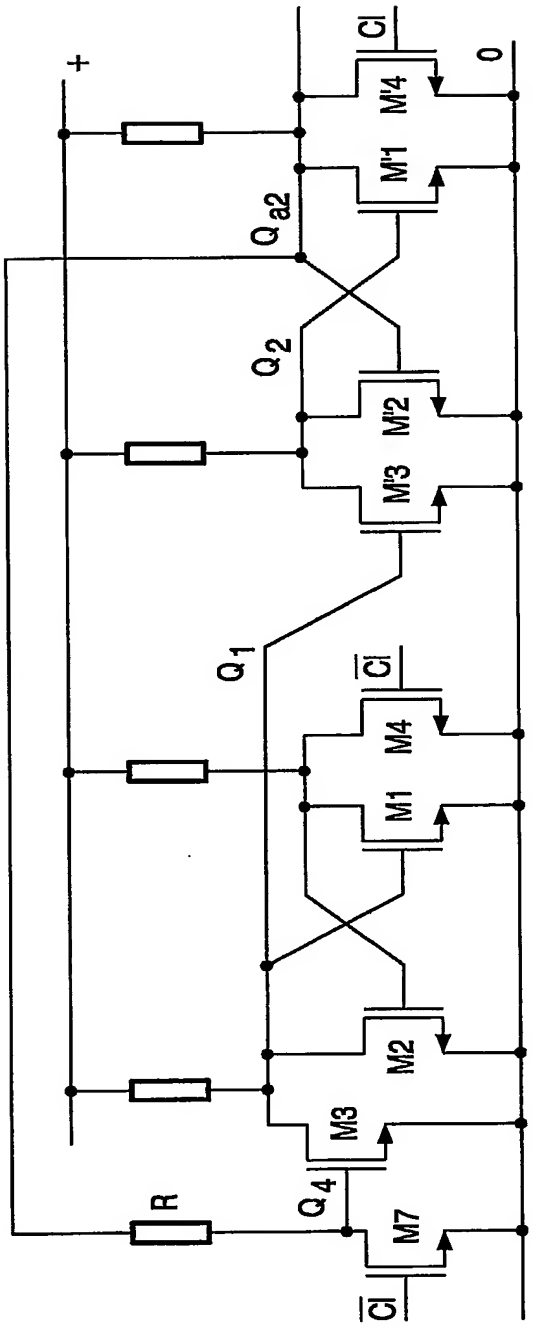

FIG. 4